Case No.: NORTH-395A/A-2240

RADIO TAG FOR LFM RADAR

CROSS-REFERENCE TO RELATED APPLICATIONS

(Not Applicable)

STATEMENT RE: FEDERALLY SPONSORED RESEARCH/DEVELOPMENT

(Not Applicable)

BACKGROUND OF THE INVENTION

[0001] A basic transponder receives a signal from a SAR (synthetic-aperture radar), and then retransmits the signal back to the SAR. The problem with retransmitting the signal back to the SAR without any changes is that the signal must compete with ground reflection noise from natural and cultural ground clutter. If no type of modulation is used, then to stand out above the background noise, extra power and electronics are often needed to increase the gain in the return signal, often requiring two antennas, one for receiving and one for transmitting. Most transponders do not provide any added information in the retransmitted signal. In most cases the interrogator is a SAR located in an aircraft or satellite, and a transponder is located some distance away from the radar, normally on the ground.

[0002] The ability to provide command control and communications to and from a transponder has many potential applications. Besides the military applications for battlefield management, intelligence gathering and the like, there are commercial applications which include

transponder status, other environmental status and emergency response. A RFID (radio frequency identification) system contains two main elements, an interrogator and one or more transponders. In the radar transmission between the interrogator and transponder, a RF signal is encoded within the SAR pulse to provide information between the interrogator and transponder, that is normally unknown to the other element.

[0003] U.S. Patent 5,486,830 discloses a RFID system wherein digital codes are encoded in the SAR signal that is received by a transponder, also called a RF tag or simply tag. A single antenna can be utilized by this transponder to transmit and receive signals. This is accomplished by a time-gating method using a 50% duty cycle factor for setting the tag's transmitting and receiving intervals, which are mutually exclusive. The received SAR signal is mixed with a reference oscillator to provide a detected signal that can be decoded. Tag logic and timing circuits measure the time between detected pulses and decode these pulses into downlink commands from the SAR, symbols of the downlink commands are encoded in the spacing between the SAR pulses. Downlink commands contain mode information that allows the SAR and tag to obtain a common pulse index (coarse synchronization). However, in order to achieve fine synchronization the tag must average the measured time-of-arrival of a number of pulses. After fine synchronization is achieved, and if so commanded, the tag will go into the uplink mode. The tag device phase encodes its echo with a sequence containing both prescribed and periodic or pseudo-random patterns, containing status or information unknown to the radar source's signal processor. A bi-phase (0/pi) modulator is utilized to allow selective amplification of +1 or -1 of the signal before retransmitting the signal back to the SAR. The signal

processing at the SAR mixes a sequence identical to the prescribed periodic or pseudo-random selective amplification against the received echoes. This selective amplification spreads the spectrum of the natural or cultural echoes and de-spreads the tag's echo, making the retransmitted signal stand out above the natural or cultural noise.

SUMMARY OF THE INVENTION

[0004] The present invention is an improvement over the other RFID systems. Prior art used simple pulses defined by their spacings in the SAR pulses. The pulses represent symbols that encode the digital information contained in the SAR pulses.

[0005] The present invention uses SAR LFM (linear frequency modulation) pulse waveforms. One advantage of using LFM pulse waveforms is that these waveforms are not noise sensitive. While the symbols of the encoded digital code are determined by the time internal between the pulses as in U.S. Patent 5,486,830, noise can cause an incorrect interval to be detected and thereby generate an invalid message.

[0006] Two receivers, an AM and a FM receiver, are connected to an antenna and are used to demodulate their respective components of the LFM pulse waveform. The output of the AM receiver is the demodulated envelope that is proportional to the amplitude of the AM component of the LFM pulse waveform. The amplitude and time duration are compared to a preprogrammed threshold and time duration criteria. The preprogrammed criteria are stored in the tag DSP (Digital Signal Processor. If both the threshold value and time duration are determined to be valid, then the demodulated FM portion of the LFM pulse waveform is checked for validity.

[0007] A reference local oscillator is needed to demodulate FM signal component of a LFM pulse waveform. This is generated by delaying LFM pulse waveform and mixing it with the non-delayed LFM pulse waveform. A separate reference oscillator is, therefore, not required. The demodulated waveform is then passed through a zero-crossing detector. The output of the zero-crossing detector is sampled and the samples are counted by the DSP to estimate the average frequency over the pulse duration.

[0008] In order to determine the slope of the frequency deviation, a 90°power splitter is added to the local oscillator, before the mixer. The power splitter has two outputs, one in-phase and one in quadrature-phase with the LFM pulse waveform. The signal component set of mixer, lowpass filter, zero-crossing detector and sampler is replaced with two identical sets of components. The output of the set with the in-phase signal is labeled "FM In-Phase", and the output of the set with the quadrature-phase signal is labeled "FM quadrature-phase". These two outputs are then used by the DSP to determine the slope of the frequency deviation.

[0009] The DSP utilizes the slope information and frequency deviation to determine the message sent by the SAR. Though the use of Phase Modulation (PM), the tag can encode data to send back to the SAR.

[0010] By using RF switches, the signals can be directed so that the same antenna can be used for receiving and transmitting. Since the same antenna is used, a chop timing of the RF switches in required. There are 3 stages in the chop signal: receive, transmit and blanking. The blanking stage is required to prevent oscillations in the tag due to reflections from nearby objects. Some systems require randomizing the blanking time to prevent the radar from accidentally locking onto the spectral lines that are

generated during the chopping of the RF signal. The blanking times can change pseudo-randomly each cycle.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Illustrative and presently preferred embodiments of the present invention are shown in the accompanying drawings in which:

[0012] Figure 1 is simplified block diagram of the tag;

[0013] Figure 2 is the detailed block diagram of the tag;

[0014] Figure 3 is the detailed block diagram of the digital signal processor;

[0015] Figure 4 is the software flow diagram during message reception;

[0016] Figure 5 is the signal flow through the AM receiver;

[0017] Figure 6 is the signal flow through the FM receiver;

[0018] Figure 7a is a graph of the low pass filter output of the FM receiver;

[0019] Figure 7b is a table showing the frequency estimator code;

[0020] Figure 8 is a timing diagram for synchronizing the tag and radar;

[0021] Figure 9 is the signal flow during transmit;

[0022] Figure 10 shows the chop timing of S1 and S2;

[0023] Figure 11a is a diagram of the random chop generator;

[0024] Figure 11b is a table showing the tag modulation states per pulse;

[0025] Figure 12 shows the tag modulation.

[0026] Figure 13a shows the FM receiver without slope direction;

[0027] Figure 13b shows the FM receiver with slope direction capability;

[0028] Figure 14a shows a graph of the I and Q outputs of the FM Receiver;

[0029] Figure 14b is a table showing the slope measurement code;

[0030] Figure 15 shows the slope polarity of a positive-going LFM; and

[0031] Figure 16 shows the slope polarity of a negative-going LFM.

DETAILED DESCRIPTION

[0032] Figure 1 shows the transponder device or tag 10 simplified block diagram. An antenna 1 receives the LFM (linear frequency modulation) input waveform from SAR. The received waveform is then fed into the AM receiver 2, the FM receiver 3, and a storage element 6. The AM receiver 2 demodulated output signal is then fed into the digital signal processor (DSP) 4. If the DSP 4 determines that the AM demodulated output signal is valid, then the DSP 4 determines if the demodulated output of the FM receiver 3 is valid. If both demodulated outputs are valid, then the DSP 4 checks the validity of the received LFM input waveform against stored data. After the DSP 4 has determined that the data encoded in the LFM input waveform is valid, and decoded the message; the RF signal stored in the storage element 6 is modulated in the modulator 5. The output of the modulator 5 is then fed back into the antenna 1 to be transmitted back to the originating source.

[0033] Figure 2 shows a further breakdown of the components of the tag 10. The typical operating frequency is 8 to 12 GHz. The LFM input waveform is sensed in antenna 1. A bandpass filter 11 is utilized to remove any undesirable out of band signals out of the LFM input waveform. A first directional coupler 12 passes the filtered LFM input waveform to a RF switch 13 through the

coupled side of the directional coupler 12. If switch 13 is closed, then the received filtered RF signal will be fed into a low noise amplifier 14. The RF switch 13 is only closed during the receive cycle. Switch 20 is open during the receive cycle. The RF filtered LFM input waveform is then routed through the coupled side of the second coupler 15. A second low noise amplifier 22 amplifies the signal, which is then fed into a power splitter 23. Up to the input of the power splitter 23, the LFM input waveform signal has been identically processed for both the AM receiver 2 and FM receiver 3.

[0034] The signal flow in the AM receiver 2 continues from the output of the power splitter 23 though the bandpass filter 24. Bandpass filter 24 removes unwanted out of band noise generated by the two previous amplifier stages 14 and 22. The output of filter 24 is applied to a diode detector 25. The detector 25 demodulates the envelope of the LFM input waveform; the output of detector 25 is proportional to the amplitude of the LFM input waveform. A square law device is used in the detector although other types of detector devices are possible, such as envelope, synchronous, and log-video; however the square law detector is one of the most common forms. In the preferred embodiment, the detector 25 consists of a tunnel diode and passive bias components and the design is not shown but is well known to practitioners of the art. The detected output of the detector 25 is filtered by a low pass filter 26, which removes the higher order frequency terms which were generated during the non-linear process of detection. A video amplifier 27 amplifies the filtered output of filter 26. The output of the video amplifier 27 is applied to the positive input terminal of a threshold comparator 28. The voltage at the negative input terminal of the comparator 28 is set by a digital to analog

converter (DAC) 35. The output of the DAC 35 is determined by the digital word from the DSP 4. The output of the comparator 28 is a digital logic "1" when the input at the positive input terminal is higher than the voltage at the negative input terminal. The output of comparator 18 is a logic "0" when the input at the positive input terminal is lower than the voltage at the negative input terminal. The output of the comparator 28 is labeled "AM After Threshold Detection" in Figure 2 and is applied to a field programmable gate array (FPGA) 44 contained in DSP 4 shown in Figure 3. The FPGA 44 measures the pulse width of the comparator 28 output. This pulse width is screened to be within the programmable minimum and maximum limits, which typically range between 10μs to 150μs. A pulse width, that does not pass the pulse width screening, will not enable the frequency estimator within the DSP 4, as shown in Figure 4, the tag software flow diagram. An invalid pulse will cause no action in the frequency estimator. Only after a pulse width has passed the pulse width screening will the frequency estimator be enabled.

[0035] The signal flow in the FM receiver 3 continues from the output of the power splitter 23 though the low noise amplifier 29. The FM receiver shares common parts with the AM receiver 2 from the antenna 1 to the input of power splitter 23 as illustrated in Figures 2, 5 and 6. In the FM receiver is a new input signal labeled "LO" (Local Oscillator) which is utilized as shown in Figure 6. This signal is generated from the input LFM pulse waveform that shares common parts with the AM receiver and FM receiver from the antenna 1 to the input of the second directional coupler 15, as illustrated in Figures 2, 5 and 6. At the coupler 15, the signal passes through the main line of second directional coupler 15, and then through the delay line 16. The time delay, of the delay line 16, in the

preferred embodiment is 60ns with the delay element being a coaxial cable. However, the design of the delay line 16 will operate with any delay as long as the delay is constant over frequency. Other delay elements can be used such as SAW, BAW, optical fiber, tuned filter and digital circuits such as DRFM. These alternate delay elements may require support circuits that are not shown here, but are well known in the art. The output of delay line 16 then passes through the coupled side of the third directional coupler 17. The output of the third directional coupler 17 then passes through the LO low noise buffer amplifier 34. The output of the buffer amplifier 34 is then fed into the LO input of the mixer 30.

[0036] The LO signal at the mixer 30 input is a delayed replica of the LFM input waveform received at the antenna 1. This LO signal and the mixer 30 comprise the frequency detector in the FM receiver 3 of the original LFM pulse waveform. The frequency demodulation is accomplished by multiplying the delayed signal (LO) with the non-delayed signal in the mixer 30. The formula for the demodulation output of the low pass filter 31 after the mixer 30, for an LFM input, is given below:

[0037] Frequency output (Hz) = delay (seconds) X LFM (Hz/second).

[0038] The following is an example calculation of the above formula. The tag has a time delay of 60ns, and an input LFM waveform is applied at 8.5 GHz with a positive-slope ramp deviation of 100 MHz and a pulse width of 27.7μs. The frequency output is 60e-9 x 100e6/27.7e-6 or approximately 216 KHz. Figure 7 shows the output of the low pass filter 31 for this input signal.

[0039] After the low pass filter 31, the FM signal is limited with a zero-crossing comparator 32 that converts the signal into a one bit digital value and the sampling of

the one bit digital value is controlled by the Sample Clock input, from the FPGA 44 of the DSP 4 as shown in Figure 3, to the sampler 33. Sampler 33 may be a clocked register or an other circuit that can hold the value of the digital bit until the next sample clock is received by the sampler 33. The output of sampler 33 is labeled "LFM After Sampling". The output of sampler 33 is applied to the microprocessor 42 in the DSP 4 in Figure 3, for storage in the memory RAM 41 for further processing by the microprocessor 42. It is only processed if the output of comparator 28 is within the preprogrammed valid range of widths.

[0040] Figure 4 is a diagram of the processing steps of the microprocessor. The output of the FM receiver 3, which is the output of the sampler 33, is fed into the microprocessor 42 for frequency estimating. The frequency estimator counts the zero-crossings of the demodulated FM signal from the output of sampler 33, and calculates the average frequency during the valid receive interval. The code for this frequency estimator is provided in Figure 7B. In Figure 7B, the variable "SS" represents a valid receive interval. If the variable "SS" is not equal to 1, then the output of the threshold comparator 28 is not a digital logic 1. All received signals that do not generate a digital logic 1 at the output of comparator 28 are considered to be noise and are not processed further. The variable "SLIN" is the digital bit in the output signal or comparator 33 labeled as "FM After Sampling". The variable "clock" is a 2MHz sample clock. The actual frequency can be changed but the program must make the variable "clock" equal to the actual sample clock rate used. The variable "data" is the sample length. The sample length dynamically changes with the width of the input pulse.

[0041] In the previous example, the sample length would

be 2Mhz x 27.7μs, or approximately 55 samples. Using the frequency estimator of Figure 7B and the 100 MHz deviation from the example, the calculated frequency output is 219KHz. This is within 2% of the theoretical value of 216KHz and is satisfactory for the RFID system. The FM processing continues in Figure 4, where the measured frequency is compared to a table of valid frequencies. If the comparison is true, then the tag builds a message from the data that was encoded in the pulse width and frequency deviations of the received input LFM pulse waveform. Although this implementation is described in software, faster operation could be obtained using a matched filter in the DSP section.

[0042] The tag 10 checks the validity of the data in the message by examining the data fields and performing a checksum. An example of a checksum is the CCITT 16 bit CRC (cyclic redundancy check). However, other types of checksum may be used since the type of checking does not materially affect the performance of the tag. The tag's 10 checksum is compared with the transmitted checksum and if they match then the message is valid and the tag declares Message Complete. A valid message will typically contain the radar pulse width, radar PRI, and transmitted checksum, and may include other information for the tag 10 or about the radar depending on the system operation.

[0043] A valid message will enable data transmission from the tag 10. The tag 10 must align its transmission so that its pulse is on top of, or synchronous with, the radar pulse. The tag 10 does this by loading the initial radar pulse width and radar PRI (pulse repetition interval) in a counter of the DSP 4, but not starting the counter. These values in the counter are the pulse width and PRI from the valid message that were obtained after the tag declares Message Complete. At the starting edge of the initial

radar pulse, a digital control signal, download_intn, is generated, which is a request by the FPGA 44 to the microprocessor 42 for modulation data. This data is used in the validating of any decoded valid AM and FM demodulated output to the DSP 4. From the data decoded from the initial SAR pulse, the tag 10 estimates when the next pulse will be received. The exact timing for the ld_symbol during the initial pulse is not critical, however the ld_symbol must occur before the first transmit pulse. The download_intn is a request from the FPGA 44 to the microprocessor 42 for new modulation data. This data is used in the next pulse one PRI later. Ld_symbol latches the modulation data into the FPGA 44 before rf_detect occurs. The tag 10 waits for the leading edge of the initial radar pulse and when it detects the leading edge it transmits after the initial PRI. During the following pulses the tag loads the counter with the actual radar PRI and so transmits this PRI repeatedly. The PRI timer gets resynchronized to each incoming RF to take into account inaccuracies in the FPGA clock. After the initial PRI, an uplink gate signal is generated to control the waveform XMT, which is the envelope of the RF transmission from the tag. In this way the tag 10 becomes synchronized with future pulses from the radar. The error between the tag pulse and radar pulse is typically less than ± 100ns. The process of synchronizing the tag with the radar is illustrated in Figure 8. The following is a description of the signals named in the figure:

[0044] •"rf" is the envelope of the received RF signal in the LFM pulse waveform;

[0045] •"latency" is the time delay from the received RF to the digital output of the threshold detector 28, labeled

as "AM After Threshold Detector", and occurs due to circuit delay in the AM receiver 2;

[0046] •"init_pri" is the initial PRI transmission from the tag 10;

[0047] •"gate" is the width of the received LFM pulse waveform;

[0048] •"pri" is the PRI of the received LFM pulse waveform, and the PRI of all tag transmissions except for the initial PRI;

[0049] •"rf_detect" is the same as the output of the threshold detector 28, labeled as "AM After Threshold Detector";

[0050] •"uplink gate" is the pulse width of the tag transmission;

[0051] •"download_intn" is a digital word signal sent by the FPGA 44 to the microprocessor 42 and is a request to the microprocessor 42 for modulation data;

[0052] •"ld_symbol" initializes the FPGA 44 with new modulation information from the microprocessor 42;

[0053] •"xmt" is the envelope of the RF transmission from the tag 10;

[0054] •"chopping signal" refers to a toggling state of the controlling signals S1 and S2 that control RF switch S1 13 and RF switch S2 20 respectively.

[0055] The LFM pulse waveform signal flow during

transmit is shown in Figure 9. The dashed line was previously described in the received signal flow and is also part of the transmission. The LFM input pulse waveform uses the same components as the AM 2 and FM 3 receivers up to the input of the second directional coupler 15. The LFM pulse waveform signal passes through the main line of second directional coupler 15, followed by the delay line 16. It then passes through the main line of third directional coupler 17. The LFM pulse waveform signal that was stored in delay line 16, after passing through the directional coupler 17 is electrically coupled to the variable attenuator 18, phase modulator 19, RF switch S2 20 (closed in transmit), power amplifier 21, back through the main line of the first directional coupler 12 and through bandpass filter 11 and transmitted from the antenna 1.

[0056] To allow the tag to share the same antenna 1 for both receive and transmit, the chopping signals S1 and S2 use the same frequency and the length of delay for the delay line 16 is based on the frequency used in the timing of chopping signals S1 and S2. The timing of S1 and S2 is shown in Figure 10 for a 60ns delay line 16. In this figure the receive time is 60ns, transmit time is 60ns, and the blanking time (when the tag is neither transmitting nor receiving) is 60ns. The transition time from on to off and vice versa due to the RF switches S1 13 and S2 20 is 10ns. A complete cycle in the example in Figure 10 is 180ns. The blanking interval in Figure 10 prevents oscillations due to reflections from nearby objects.

[0057] Some systems require randomizing the blanking time to prevent the radar from accidentally locking onto the spectral lines that are generated during the chopping of the RF signal. The randomizing circuit for chop timing is shown in Figure 11a. The blanking time changes pseudo-

randomly each cycle from 60ns to 200ns with a resolution of 20ns. The design is a [7,1] maximal length generator and the initial seed is binary 1111111. The sequence repeats every 127 chop cycles. The circuits for the chop timing and chop randomization are contained in the FPGA 44. Other randomizing circuit designs could also be utilized.

[0058] The pulse is modulated with tag data using the signal phase modulator 19 as shown in Figure 2, by the signal labeled "PM". The phase modulator 19 is a 5-bit phase shifter and is capable of placing frequency modulation and phase modulation on the RF signal. A typical modulation consists of a linear frequency slope and a bi-phase value. During the process of modulation, the binary data in the message is encoded. An example of an encoding scheme is shown in Figure 11b Three bits of data from the tag are placed on each pulse using different states of frequency deviation and phase. However, the tag is capable of generating other modulation values, and the design is capable of a broad range of frequency and phase modulation.

[0059] The RF output from the tag 10 for the example in Figure 11b is shown in Figure 12. It shows that the tag adds chop modulation, phase modulation, and linear frequency modulation (LFM) to the radar pulse. The transmit time of the tag is synchronous with the radar pulse. The plus symbol in the LFM+ indicates that the tag has modified the LFM slope of the original radar LFM signal.

[0060] The tag adjusts the gain in the transmit path using the AM signal at the variable RF attenuator 18 in Figure 2, the signal being generated from the microprocessor 42 in Figure 3. The AM signal controls a 5-bit digitally tunable RF attenuator. However, the signal may also be an analog voltage in another implementation and

the type of RF attenuator does not materially affect the tag 10. The microprocessor 42 sets the amplitude value of the AM. The gain is typically set to 63dB (peak) as measured from the antenna RF input to the antenna RF output.

[0061] Figure 13a is a partial block diagram of the FM receiver 3 in Figure 2. These components can not distinguish between increasing and decreasing LFM signals, because they respond equally to positive and negative slopes from the FM signal. The preferred embodiment uses a mixer 30, followed by a low pass filter 31, a zero-crossing detector 32 and a sampler 33. The output of the sampler 33 is labeled LFM After Sampling. This output is then processed by the microprocessor 42 in the DSP 4.

[0062] This restriction is overcome by quadrature detection and processing of the I and Q signals as shown in Figure 13b of Figure 13. Figure 13b shows the block diagram of the revised design for calculating the slope. The amplifiers 29 and 34 are unchanged from the preferred embodiment. A 90° power splitter 100 is now placed between the output of amplifier 34 and mixer 30. The 90° power splitter 100 produces two outputs, one is in-phase with the input signal and the other output is out of phase by 90° and is in quadrature-phase with the input. Each output is processed by a separate but identical set of components. The outputs of the two sets of components are labeled "FM In-Phase" (I) and "FM Quadrature-Phase" (Q). The output from the revised FM receiver 3 labeled "FM in-phase" uses the component set: mixer 30I, lowpass filter 31I, zero-crossing detector 32I and sampler 33I. The output from the revised FM receiver 3 labeled "FM Quadrature-Phase" uses the component set: mixer 30Q, lowpass filter 31Q, zero-crossing detector 32Q and sampler 33Q.

[0063] These two output signals are further processed by

the microprocessor 42 in the DSP4, to find the polarity of the slope. The analog outputs of I and Q prior to digitizing are shown in Figure 14a, using the same input example as previously discussed.

[0064] The processing steps for the slope polarity are shown in Figure 14b. SLOPE[n] is the output and is initialized to zero. The result is +1 when the slope is positive and -1 when the slope is negative. The data processing is accomplished by the microprocessor 42 inside the DSP 4. The output of the slope polarity is shown in Figure 15 for the positive slope of the example. The top trace is the detection output of the AM receiver 2 threshold comparator 28 and is shown for reference only, and the bottom trace is the slope polarity scaled by ½. Figure 16 is the output for a negative slope.

[0065] The algorithm in Figure 14b provides multiple outputs, separated in time but having identical value, and any one of the multiple values is suitable for defining polarity. Typically the microprocessor 42 will select the first value. The number of multiple values is a function of the input FM deviation and pulse width.

[0066] The above teachings are illustrations of preferred embodiment of the present invention. It should be noted that modifications to the invention, such as would occur to those of ordinary skill in the art, are also within the intended scope of the present invention.